WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of memory cells each of which includes a first MOS transistor with a charge accumulation layer and a control gate and a second MOS transistor having one end of its current path connected to one end of a current path of the first MOS transistor;

a memory cell array which has the memory cells arranged in a matrix in such a manner that the memory cells adjoining in the column direction share the other ends of the current paths of the first MOS transistors or the other ends of the current paths of the second MOS transistors;

bit lines each of which connects commonly the other ends of the current paths of the first MOS transistors of the memory cells in the same column;

word lines each of which is formed by connecting commonly the control gates of the first MOS transistors of the memory cells in the same row;

select gate lines each of which is formed by connecting commonly the gates of the second MOS transistors of the memory cells in the same row;

a column decoder which selects any one of the bit lines;

a first row decoder which selects any one of the word lines;

a second row decoder which selects any one of the

select gate lines; and

first metal wiring layers which are provided for every select gate lines, each of which is formed in the row direction so as to pass through almost the central part of the memory cells, is connected electrically to the corresponding one of the select gate lines, and transmits a row select signal for the second row decoder to select the select gate line.

2. The semiconductor memory device according to claim 1, wherein each of the first metal wiring layers is formed above a region between the central part of the select gate line and the central part of the word line.

3. The semiconductor memory device according to claim 1, further comprising:

first contact plugs which are connected to the gates of the second MOS transistors;

second metal wiring layers which are provided for every first contact plugs and are connected electrically to the first contact plugs; and

second contact plugs each of which is formed on a region of the second wiring layer between the central part of the select gate line and the central part of the word line and is connected to the first metal wiring layer.

4. The semiconductor memory device according to claim 3, wherein each of the second metal wiring layers

is extended from the upper region of the gate of the second MOS transistor connected to the corresponding one of the first contact plugs toward the upper region of the control gate of the first MOS transistor connected to the second MOS transistor.

5. The semiconductor memory device according to claim 3, wherein the memory cell array includes:

a plurality of first regions each of which includes two or more of the memory cell columns; and

second regions each of which is provided between the first regions adjacent to each other,

the second metal wiring layers and the first and second contact plugs are formed in the second regions, and

the select gate line is connected to the second metal wiring layers in the second region.

6. The semiconductor memory device according to claim 5, further comprising:

third contact plugs each of which is connected to the other ends of the current paths of the first MOS transistors in the first region;

third metal wiring layers which are provided for every third contact plugs and are connected to the third contact plugs; and

fourth contact plugs which connect the third metal wiring layers to the bit lines, wherein

the second metal wiring layers have almost the

same width in the row direction as the third metal wiring layers.

7. The semiconductor memory device according to claim 5, further comprising:

a source line which connects commonly the other ends of the current paths of the second MOS transistors; and

fourth metal wiring layers which are formed in the column direction at a level higher than the source line and are connected to the source line by fifth contact plugs, wherein

the source line includes first wiring regions each of which connects commonly the other ends of the current paths of the second MOS transistors of two or more of the memory cells in the same row and a second wiring region which connects the first wiring regions in the column direction,

each of the first regions includes a third region which includes one of the memory cell columns,

the second wiring region of the source line and the third metal wiring layer are formed in the third region, and

the source line is connected to the third metal wiring layer in the third region.

8. The semiconductor memory device according to claim 7, wherein the fourth metal wiring layers are located at the same level as the bit lines.

9. The semiconductor memory device according to claim 7, wherein the fourth metal wiring layers have the same width as the bit lines.

10. The semiconductor memory device according to claim 7, wherein the first wiring regions of the source line adjacent to each other with the second region between them are isolated from one another in the row direction, and

the first metal wiring layers adjacent to each other with the second region between them are connected commonly in the row direction via the second region.

11. The semiconductor memory device according to claim 1, further comprising:

a source line which connects commonly the other ends of the current paths of the second MOS transistors;

wherein the source line includes a first wiring region which connects commonly the other ends of the current paths of the second MOS transistors of two or more of the memory cells in the same row.

12. The semiconductor memory device according to claim 11, wherein the source line further includes a second wiring region which connects the first wiring layers in the column direction.

13. The semiconductor memory device according to claim 11, further comprising:

fourth wiring layers which are formed in the

column direction at a level higher than the source line and are connected to the source line by fifth contact plugs.

14. A semiconductor memory device comprising:

a plurality of memory cells each of which includes a first MOS transistor which includes a charge accumulation layer and a control gate;

a memory cell array which has the memory cells arranged in a matrix;

bit lines each of which connects commonly the drain regions of the first MOS transistors of the memory cells in the same column;

word lines each of which is formed by connecting commonly the control gates of the first MOS transistors of the memory cells in the same row;

a source line which electrically connects commonly the source regions of the memory cells and which includes a first wiring region electrically connecting the source regions of the first MOS transistors of the memory cells in the same row commonly and a second wiring region connecting the first wiring regions in the column direction;

a column decoder which selects any one of the bit lines; and

a first row decoder which selects any one of the word lines.

15. The semiconductor memory device according to

claim 14, further comprising:

first metal wiring layers which are formed in the column direction at a level higher than the source line and are connected to the first and second wiring regions of the source line by first contact plugs.

16. The semiconductor memory device according to claim 15, wherein the first metal wiring layers are located at the same level as the bit lines.

17. The semiconductor memory device according to claim 15, wherein the first metal wiring layers have the same width as the bit lines.

18. The semiconductor memory device according to claim 15, wherein the memory cell array includes:

a plurality of first regions each of which includes a plurality of memory cell columns; and

second regions each of which is provided between the first regions adjacent to each other and includes one of the memory cell columns,

the second wiring regions of the source line and the first metal wiring layer are formed in the second region, and

the source line is connected to the first metal wiring layer in the second region.

19. The semiconductor memory device according to claim 18, wherein each of the memory cells further includes a second MOS transistor having a drain connected to the source region of the first MOS

transistor, and

the source line connects commonly the source regions of the second MOS transistors, and

the device further includes:

select gate lines each of which is formed by connecting commonly the gates of the second MOS transistors of the memory cells in the same row;

a second row decoder which selects any one of the select gate lines;

second metal wiring layers which are provided for every select gate lines and each of which is connected electrically to the corresponding one of the select gate lines and transmits a row select signal for the second row decoder to select the select gate line;

second contact plugs connected to the gates of the second MOS transistors;

third metal wiring layers which are provided for every second contact plugs and are connected electrically to the second contact plug; and

third contact plugs which are formed on the third metal wiring layers so as to be connected to the second metal wiring layers, the first regions including third regions, the third metal wiring layers and the second and third contact plugs being formed in the third region, the select gate lines being connected to the second metal wiring layers in the third region.

20. The semiconductor memory device according to

claim 19, wherein each of the third metal wiring layers is extended from the upper region of the gate of the second MOS transistor connected to the corresponding one of the second contact plugs toward the upper region of the control gate of the first MOS transistor connected to the second MOS transistor.

21. The semiconductor memory device according to claim 19, wherein each of the third contact plugs is formed on a region of the second wiring layer between the central part of the select gate line and the central part of the word line.

22. The semiconductor memory device according to claim 19, wherein the memory cells arranged in a matrix in the memory cell array are arranged in such a manner that the memory cells adjacent to one another in the column direction share the drain regions of the first MOS transistors or the source regions of the second MOS transistors, and

each of the second metal wiring layers is formed above a region between the central part of the select gate line and the central part of the word line and passes through almost the central part of the memory cells.

23. The semiconductor memory device according to claim 19, wherein the first wiring regions of the source line adjacent to each other with the second region between them are isolated from one another in

the row direction, and

the second metal wiring layers adjacent to each other with the second region between them are connected commonly in the row direction via the second region.

24. The semiconductor memory device according to claim 18, further comprising:

fourth contact plugs which are connected to the drain regions of the first MOS transistors in the first regions;

fourth metal wiring layers which are provided for every fourth contact plugs and are connected to the fourth contact plugs; and

fifth contact plugs which connect the fourth metal wiring layers to the bit lines, wherein

the third metal wiring layers have almost the same width in the row direction as the fourth metal wiring layers.

25. The semiconductor memory device according to claim 14, wherein each of the memory cells further includes a second MOS transistor having a drain region connected to the source region of the first MOS transistor,

the source line connects commonly the source regions of the second MOS transistors and

the device further includes:

select gate lines each of which is formed by connecting commonly the gates of the second MOS

transistors of the memory cells in the same row connected commonly;

a second row decoder which selects any one of the select gate lines; and

first metal wiring layers which are provided for every select gate lines and each of which is connected electrically to the corresponding one of the select gate lines and transmits a row select signal for the second row decoder to select the select gate line.

26. The semiconductor memory device according to claim 25, further comprising:

first contact plugs connected to the gates of the second MOS transistors;

second metal wiring layers which are provided for every first contact plugs and are connected electrically to the first contact plugs; and

second contact plugs which are formed on the second metal wiring layers and are connected to the first metal wiring layers.

27. The semiconductor memory device according to claim 26, wherein each of the second metal wiring layers is extended from the upper region of the gate of the second MOS transistor connected to the corresponding one of the first contact plugs toward the upper region of the control gate of the first MOS transistor connected to the second MOS transistor.

28. The semiconductor memory device according to

claim 26, wherein each of the second contact plugs is formed on a region of the second wiring layer between the central part of the select gate line and the central part of the word line.

29. The semiconductor memory device according to claim 25, wherein the memory cells arranged in a matrix in the memory cell array are arranged in such a manner that the memory cells adjacent to one another in the column direction share the drain regions of the first MOS transistors or the source regions of the second MOS transistors, and

each of the first metal wiring layers is formed above a region between the central part of the select gate line and the central part of the word line and passes through almost the central part of the memory cells.

30. The semiconductor memory device according to claim 25, wherein the first wiring regions of the source line adjacent to each other with the second region between them are isolated from one another in the row direction, and

the second metal wiring layers adjacent to each other with the second region between them are connected commonly in the row direction via the second region.